IN THE CLAIMS:

Please amend Claims 1 and 6 as follows:

1. (Four Times Amended) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining lightly doped first drain and source diffusion layers;

(d) at least one sidewall covering said gate electrode therewith; and

(e) heavily doped second drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and four lateral sides,

said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a horizontal surface of said semiconductor substrate in at least one of regions below which at least one of said second drain and source diffusion layers are to be formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said lateral surface of said sidewall,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset.

6. (Four Times Amended) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate, said gate electrode and said insulating film defining lightly doped first drain and source diffusion layers;

(d) at least one sidewall covering said gate electrode therewith;

(e) heavily doped second drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode and aligned with said at least one sidewall covering, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and four lateral sides, said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a horizontal surface of said semiconductor substrate in at least one of regions below which at least one of said second drain and source diffusion layers are formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said lateral surface of said sidewall; and

(f) low-resistive wiring layers formed at surfaces of said drain and source diffusion layers, said low-resistive wiring layers being located outwardly beyond a peripheral edge of at least one of said sidewall and said sidewall offset in said at least one of said drain and source diffusion layers,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset.